CLAIMS

Please amend the Claims as follows:

1. - 23. (Canceled).

24. (Currently Amended) ~~The computer system as recited in claim 23,~~ A computer system, comprising:

a channel unit comprising a counter corresponding to a data channel;

a processor coupled to receive computer program instructions and a power control signal, wherein the processor is configured to execute the received computer program instructions, and wherein the processor comprises at least one component that is not used when the processor has executed all received computer program instructions and is waiting for further computer program instructions, and wherein the processor is configured to transition the at least one component to a low power mode in response to the power control signal;

means for decrementing a count stored in the counter when the processor executes an instruction corresponding to the data channel;

means for producing the power control signal in the event the count stored in the counter reaches a predetermined value;

wherein the channel unit is configured to decrement the count stored in the counter when the processor executes an instruction corresponding to the data channel; and

wherein the processor is configured to provide a signal to the channel unit in the [[even]]event an instruction corresponding to the data channel is executed, and wherein the channel unit is configured to produce a wait signal in the event the count stored in the counter reaches the predetermined value.

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25. (Previously Presented) The computer system as recited in claim 24, further comprising an instruction issue unit coupled to receive computer program instructions and the wait signal produced by the channel unit, wherein the instruction issue unit is configured to provide the computer program instructions to the processor and to respond to the wait signal by producing the power control signal.

CLAIMS

Please amend the Claims as follows:

1. – 23. (Canceled).

24. (Currently Amended) ~~The computer system as recited in claim 23,~~ A computer system, comprising:

a channel unit comprising a counter corresponding to a data channel;

a processor coupled to receive computer program instructions and a power control signal, wherein the processor is configured to execute the received computer program instructions, and wherein the processor comprises at least one component that is not used when the processor has executed all received computer program instructions and is waiting for further computer program instructions, and wherein the processor is configured to transition the at least one component to a low power mode in response to the power control signal;

means for decrementing a count stored in the counter when the processor executes an instruction corresponding to the data channel;

means for producing the power control signal in the event the count stored in the counter reaches a predetermined value;

wherein the channel unit is configured to decrement the count stored in the counter when the processor executes an instruction corresponding to the data channel; and

wherein the processor is configured to provide a signal to the channel unit in the [[even]]event an instruction corresponding to the data channel is executed, and wherein the channel unit is configured to produce a wait signal in the event the count stored in the counter reaches the predetermined value.

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25. (Previously Presented) The computer system as recited in claim 24, further comprising an instruction issue unit coupled to receive computer program instructions and the wait signal produced by the channel unit, wherein the instruction issue unit is configured to provide the computer program instructions to the processor and to respond to the wait signal by producing the power control signal.